We claim:

1. A method in the fabrication of an integrated circuit including at least one bipolar transistor and at least one MOS device comprising the steps of:
- providing a silicon substrate;
- forming an active region for the bipolar transistor and an active region for the MOS device in said silicon substrate;
- forming field isolation areas around, in a horizontal plane, said active regions;
- forming a MOS gate region on said active region for the MOS device;
- forming a layer of an electrically insulating material on said MOS gate region and on said active region for the bipolar transistor; and
- defining a base region in said active region for the bipolar transistor by means of producing an opening in said electrically insulating layer, wherein
- said opening in said electrically insulating layer is produced so that the remaining portions of the electrically insulating layer partly cover said active region for the bipolar transistor; and
- said electrically insulating layer remains on said MOS gate region to encapsulate and protect the MOS gate region during subsequent manufacturing steps.

2. The method as claimed in claim 1 wherein said electrically insulating layer is a nitride layer.

3. The method as claimed in claim 1 further comprising the step of manufacturing of a capacitor, wherein a portion of said electrically insulating layer is utilized as the dielectric in said capacitor.

4. The method as claimed in claim 1 wherein said MOS gate region is formed as a silicon layer on top of an oxide layer.

5. The method as claimed in claim 4 wherein an oxide is formed on top of the silicon layer prior to forming said electrically insulating layer.

6. The method as claimed in claim 4 further comprising the step of forming an oxide layer on top of said active region for the bipolar transistor prior to forming said electrically insulating layer.

7. The method as claimed in claim 6 further comprising the step of producing said opening also through said oxide layer on top of said active region so as to expose a portion of said active region for the bipolar transistor.

8. The method as claimed in claim 6 wherein said oxide layer, on top of which said gate polysilicon layer is formed, and said oxide layer formed on top of said active region for the bipolar transistor are formed simultaneously.

9. The method as claimed in claim 1 wherein said active region for the MOS device is ion implanted prior to the formation of said MOS gate region.

10. The method as claimed in claim 1 wherein a secondary implanted collector in said active region for the bipolar transistor and a background doping of said active region for the MOS device are formed simultaneously in an ion implantation step.

11. The method as claimed in claim 10 wherein an extrinsic base for the bipolar transistor is formed on said electrically insulating layer and partly on said active region for the bipolar transistor in said opening to thereby define an emitter opening, said extrinsic base being formed prior to said ion implantation step and being protected by photoresist during said ion implantation step.

12. The method as claimed in claim 11 wherein said extrinsic base is doped and source and drain regions are formed in said active region for the MOS device simultaneously in an ion implantation step.

13. The method as claimed in claim 12 wherein also an electrode of a capacitor or a contact layer for a substrate contact is doped in the ion implantation step, in which said extrinsic base is doped.

14. The method as claimed in claim 12 wherein a silicon oxide and silicon nitride bi-layer is formed on said doped source and drain regions to thereby prevent implanted species from diffusing out of said active region.

15. The method as claimed in claim 1 wherein said active regions for the bipolar transistor and the MOS device are formed by means of ion implantation through an oxide-nitride bi-layer.

16. The method as claimed in claim 1 wherein a collector including a collector plug for said bipolar transistor is formed, and wherein said collector plug is doped by means of ion implantation with two different dopant species of the same doping type, but which have different diffusivities, so as to achieve a low-resistive and deep collector plug.

17. The method as claimed in claim 16 wherein an emitter contact is formed, and wherein said emitter contact is doped with one of said dopant species used in said collector plug implantation.

18. The method as claimed in claim 16 wherein said ion implantation of the collector plug is performed in three separate steps, each step comprising the ion implantation of a dopant species at a set energy and a set dose.

19. The method as claimed in claim 18 wherein high resistance and low resistance resistors are formed in said three-step ion implantation.

20. The method as claimed in claim 1 wherein the bipolar transistor is an NPN-transistor and the MOS device is a PMOS transistor.

21. The method as claimed in claim 1 further comprising the steps of:
- forming a buried collector region for the bipolar transistor in said substrate, said buried collector region being located underneath said active region for the bipolar transistor;
- producing the field isolation area formed around the active region for the bipolar transistor as a shallow trench in said silicon substrate, said shallow trench extending vertically from the substrate surface and down into the buried collector region; and
- filling said shallow trench with an electrically insulating material.

22. The method as claimed in claim 21 wherein said buried collector region and said shallow trench are formed relative each other so that said buried collector region extends into areas located underneath said shallow trench.

23. The method as claimed in claim 22 wherein said buried collector region is strongly n-doped.

24. The method as claimed in claim 21 wherein a deep trench is formed in said shallow trench.

25. The method as claimed in claim 1 wherein a vertical bipolar transistor is formed in said active region for the bipolar transistor, the doping profiles and heat treatment thereof being designed to produce a transistor, which will fully deplete from its base to its subcollector at a base-collector bias voltage larger than 2 V.

26. The method as claimed in claim 1 wherein a vertical bipolar transistor is formed in said active region for the bipolar transistor, the doping profiles and heat treatment thereof being designed to produce a transistor, which will fully deplete from its base to its subcollector at a base-collector bias voltage larger than 1 V.

27. The method as claimed in claim 25 wherein the collector is formed with a retrograde doping profile.

28. The method as claimed in claim 1 wherein said integrated circuit is an integrated circuit for radio frequency applications.

29. The method as claimed in claim 1 wherein said subsequent manufacturing steps include a step of oxidation, ion implantation, or etching.

30. The method as claimed in claim 8 wherein said oxide layer, on top of which said gate polysilicon layer is formed, and said oxide layer on top of said active region for the bipolar transistor are grown.

31. The method as claimed in claim 23 wherein said buried collector region is n-doped to a concentration of at least about 1E19 cm^{-3}.

32. The method as claimed in claim 23 wherein said active region for the bipolar transistor is doped to a concentration not higher than about 1E17 cm^{-3}.

33. The method as claimed in claim 23 wherein said active region for the bipolar transistor is doped to a concentration not higher than about 1E16 cm^{-3}.

34. The method as claimed in claim 23 wherein said active region for the bipolar transistor is doped to a concentration of about 1E16 cm^{-3}.

35. The method as claimed in claim 24 wherein said deep trench is self-aligned to said shallow trench.

36. In the fabrication of an integrated circuit, a method for forming a shallow trench for isolation of a vertical bipolar transistor comprised in said circuit, comprising the steps of:
- providing a semiconductor substrate of a first doping type;
- forming a buried collector region of a second doping type for the bipolar transistor in said substrate;
- epitaxially growing a silicon layer on top of said substrate;
- forming an active region of said second doping type for the bipolar transistor in said epitaxially grown silicon layer, the active region being located above the buried collector region;
- forming a shallow trench in said epitaxially grown silicon layer and said silicon substrate, said shallow trench surrounding, in a horizontal plane, said active region and extending vertically a distance into said substrate; and
- filling said shallow trench with an electrically insulating material.

37. The method as claimed in claim 36 wherein said buried collector region and said shallow trench are formed relative each other so that said buried collector region extends into areas located underneath said shallow trench.

38. The method as claimed in claim 36 wherein said shallow trench is formed by means of masking and etching.

39. The method as claimed in claim 36 wherein said substrate doping is of p-type and said buried collector region and said active region dopings are of n-type.

40. The method as claimed in claim 39 wherein said buried collector region is strongly n-doped.

41. The method as claimed in claim 36 wherein a deep trench is formed in said shallow trench.

42. The method as claimed in claim 36 wherein said integrated circuit is an integrated circuit for radio frequency applications.

43. The method as claimed in claim 40 wherein said buried collector region is doped to a concentration of at least about 1E19 cm^{-3}.

44. The method as claimed in claim 40 wherein said active region is doped to a concentration not higher than about 1E17 cm^{-3}.

45. The method as claimed in claim 40 wherein said active region for the bipolar transistor is doped to a concentration not higher than about 1E16 cm^{-3}.

46. The method as claimed in claim 40 wherein said active region for the bipolar transistor is doped to a concentration of about 1E16 cm^{-3}.

47. The method as claimed in claim 41 wherein said deep trench is self-aligned to said shallow trench.

48. An integrated circuit comprising:

- a semiconductor substrate of a first doping type, said substrate having an upper surface;
- a vertical bipolar transistor formed in said substrate, the transistor including an active region of a second doping type, wherein an emitter and a base are formed, and a buried collector region of said second doping type, said buried collector region being located underneath the active region; and
- a shallow trench for isolation of the vertical bipolar transistor, wherein said shallow trench surrounds, as seen along the surface of the substrate, the active region of said transistor, and is filled with an electrically insulating material, wherein
- said shallow trench extends vertically from the upper surface of the substrate and down into the substrate to a depth where said buried collector region is located.

49. The integrated circuit as claimed in claim 48 wherein said buried collector region extends into areas located underneath said shallow trench.

50. The integrated circuit as claimed in claim 48 wherein said buried collector region is strongly n-doped.

51. The integrated circuit as claimed in claim 48 wherein said integrated circuit is adapted for radio frequency applications.

52. The integrated circuit as claimed in claim 50 wherein said buried collector region is doped to a concentration of at least about 1E19 cm^{-3}.

53. The integrated circuit as claimed in claim 50 wherein said active region is doped to a concentration not higher than about 1E17 cm^{-3}.

54. The integrated circuit as claimed in claim 50 wherein said active region is doped to a concentration not higher than about 1E16 cm^{-3}.

55. The integrated circuit as claimed in claim 50 wherein said active region is doped to a concentration of about 1E16 cm^{-3}.